WHAT IS CLAIMED IS:

1. A transistor comprising:

a first region of a first conductivity type;

a second region of a second conductivity type that lies over the first region;

a third region of the first conductivity type that contacts the second region; and

a fourth region of the second conductivity type that contacts the third region.

2. The transistor of claim 1 and further comprising:

a trench that extends from the top surface of fourth region through the fourth region, the third region, and partially into second region;

a layer of insulation material that contacts the trench; and

a conductive gate region that contacts the layer of insulation material and fills the trench.

3. The transistor of claim 2 wherein the conductive gate region is a region of doped polysilicon.

4. The transistor of claim 2 wherein the first, second, third, and fourth regions have a <110> crystallographic orientation.

5. The transistor of claim 2 and further comprising a plug that is formed through the first region to contact the second region.

6. The transistor of claim 5 wherein the plug is metallic.

7. The transistor of claim 5 and further comprising:

a layer of isolation material that contacts the top surface of the fourth region, the layer of insulation material, and the conductive gate region;

a gate contact formed through the layer of isolation material to make an electrical connection with the conductive gate region; and

a drain contact formed through the layer of isolation material to make an electrical connection with the fourth region.

8. The transistor of claim 2 and further comprising an insulating layer that contacts the first and second regions.

9. The transistor of claim 1 and further comprising:

a plurality of trenches that extend from the top surface of fourth region through the fourth region, the third region, and partially into second region;

a plurality of insulation layers that contact the plurality of trenches such that each trench has an insulation layer; and

a plurality of conductive gate regions that contact the plurality of insulation layers and fill up the trenches.

10. The transistor of claim 9 wherein the plurality of conductive gate regions are regions of doped polysilicon.

11. The transistor of claim 9 wherein the first, second, third, and fourth regions have a <110> crystallographic orientation.

12. The transistor of claim 9 and further comprising a plug that is formed through the first region to contact the second region.

13. The transistor of claim 10 wherein the plug is metallic.

14. The transistor of claim 10 and further comprising:

a layer of isolation material that contacts the top surface of the fourth region, the plurality of insulation layers, and the plurality of conductive gate regions;

a plurality of gate contacts formed through the layer of isolation material to make electrical connections with the conductive gate regions; and

a plurality of drain contacts formed through the layer of isolation material to make electrical connections with the fourth region.

15. The transistor of claim 8 and further comprising an insulating layer that contacts the first and second regions.

16. A method of forming a transistor with a first region of a first conductivity type, the method comprising the steps of:

forming a second region of a second conductivity type that lies over the first region;

epitaxially growing a third region that contacts the second region, the third region having the first conductivity type; and

epitaxially growing a fourth region that contacts the third region, the fourth region having the second conductivity type and a top surface.

17. The method of claim 16 and further comprising:

forming a trench that extends from the top surface of fourth region through the fourth region, the third region, and partially into second region;

forming a layer of insulation material on the fourth region, the third region, and the second region;

forming a conductive material on the layer of insulation material to fill up the trench; and

planarizing the conductive material and the layer of insulation material until the layer of insulation material has been removed from the top surface of the fourth region to form an insulation region that lines the trench and a conductive gate region that contacts the insulation region and fills up the trench.

18. The method of claim 17 wherein the conductive gate region is a region of doped polysilicon.

19. The method of claim 17 and further comprising the step of forming a plug through the first region to contact the second region.

20. The method of claim 19 wherein the plug is metallic.